REMARKS

Reconsideration of the pending application is respectfully requested on the basis of the following particulars:

1. Amendments and Support for Same

By the Response, claim 2has been amended to improve the clarity of the claim language. Specifically, the phrase "the lower limit of the packet delete area is coincident with the upper limit thercof" is amended to read "the lower limit of the packet delete area is equal the upper limit thereof". No new matter has been added. Claim 3 has been cancelled. Accordingly, claims 1-3 and 4-15 are respectfully submitted for consideration. Approval and entry of the amendments are respectfully requested.

2. Claim rejections under 35 U.S.C. §112, 1st paragraph

With respect to the rejection of claims 2-3, 5-6, and 8-9, the Examiner contends that the term "coincident with" is not defined in the specification. In response, Applicant has amended claim 2 to change "coincident with" to "equal to". Support for the amended feature of claim 2 can be found in, e.g., page 7, lines 26-28, wherein it is stated that it is possible to set the level of the packet add area to T1=T0.

With respect to claim 3, Applicant has cancelled the claim and, hence, renders the rejection of claim 3 moot.

In view of the amendments and arguments set forth above, Applicant respectfully requests reconsideration and withdrawal of the §112, 1st paragraph, rejections of claims 2-3, 5-6, and 8-9.

3. Rejection of claims 1-9 under 35 U.S.C. §103(a)

With respect to the rejection of method claims 1-6 under 35 U.S.C. §103(a) as being unpatentable over Jay (US 6,400,683) in view of Haywood (U.S. 6,987,775), and with respect to the rejection of claims 7-9 under 35 U.S.C. §103(a) as being unpatentable over Jay and Haywood in view of Tokura (US 5,400,329), Applicant respectfully traverses the rejection at

least for the reason that Jay, Haywood, and Tokura, combined or separately, fail to teach, disclose, or suggest all of the limitation recited in the rejected claims.

Claim 1 of the present invention is directed to a method of controlling a jitter buffer using a FIFO. The method includes the steps of setting a packet delete area, a packet add area, and a clock control area inside the FIFO, controlling a stored packet quantity of the FIFO to delete a specified packet when the stored packet quantity exceeds a lower limit of the packet delete area, and to always delete the packets when the stored packet quantity exceeds an upper limit of the packet delete area. The method further includes the steps of controlling the stored packet quantity of the FIFO to add a specified packet when the stored packet quantity falls below an upper limit of the packet add area, and to always add the packets when the stored packet quantity falls below a lower limit of the packet add area, raising a clock frequency when the stored packet quantity of the FIFO reaches an upper limit of the clock control area, lowering the clock frequency when the stored packet quantity of the FIFO reaches a lower limit of the clock control area, and setting the clock control area between the packet add area and the packet delete area.

As supported in, e.g., Fig. 3 of the present application, claim 10 of the present invention is directed to a device for controlling a jitter buffer 301 (e.g., FIFO). The device includes a FIFO, having an input side and an output side, that configures the jitter buffer, a packet deletion circuit 306 provided on the input side of the FIFO, a packet addition circuit 307 provided on the output side of the FIFO, and a jitter buffer control circuit 302 that includes a buffer accumulation level surveillance 303 that monitors a stored packet quantity accumulated in the FIFO, a VCO 304 that supplies to vary a reproduced clock frequency.

The device further includes a buffer control circuit 305 for controlling the operations of the FIFO and peripheral circuits thereof, and for controlling the quantity of packets accumulated in the FIFO to delete the packets from the input side of the FIFO when the stored packet quantity exceeds a lower limit of a packet delete area, and to add the packets when the stored packet quantity falls below an upper limit of a packet add area, and a decoder 308 that accepts the packets outputted from the packet addition circuit 307, and decodes frames of the packets based on the clock frequency supplied from the VCO 304.

In the control device of the presently claimed invention, the buffer control circuit controls the quantity of packets accumulated in the FIFO by controlling the packet deletion circuit to delete packets from the input side of the FIFO when the stored packet quantity

exceeds a lower limit of a packet delete area. The buffer control circuit also controls the packet addition circuit that adds the packets when the stored packet quantity falls below an upper limit of a packet add area.

As recited in amended claims 1 and 10, the packet deletion circuit is provided on the input side of the jitter buffer. The packet deletion circuit deletes specific packet according to a result of monitoring a stored packet quantity in the jitter buffer. Applicant respectfully notes that, when packet deletion is necessary, the packet deletion is performed before a packet is stored in the jitter buffer, due to the inherent nature of a FIFO and to the arrangement of the packet deletion circuit on the input side of the FIFO. Therefore, the presently claimed invention is able to reduce packets that are stored in the jitter buffer.

The packet addition circuit, on the other hand, is provided on the output side of the jitter buffer. The packet addition circuit deletes specific packet according to a result of monitoring a stored packet quantity in the jitter buffer. Applicant respectfully notes that, when packet addition is necessary, the packet addition is performed after a stored packet is output from the jitter buffer, due to the inherent nature of a FIFO and to the arrangement of the packet addition circuit on the output side of the FIFO. Thus, the presently claimed invention is able to add additional packet easily.

With respect to Jay, as acknowledged by the Examiner, although Jay describes an adaptive clock wherein a clock rate of a buffer is adjusted based on the level of the buffer, Jay fails to teach, disclose, or suggest a packet deletion circuit, a packet adding circuit, or steps of adding or deleting packets as recited Applicant's claimed invention.

To cure the deficiencies of Jay, the Examiner relies on Haywood and alleges that Haywood describes the steps of setting a packet delete area and a packet add area to delete packets when stored packet quantity exceeds an upper limit, and to add packets when stored packet quantity falls below an upper limit of the packet add area, and etc. However, Applicant respectfully asserts that Haywood describes variable FIFO that includes three memories (i.e., a tail FIFO 16, a head FIFO 17, and a large-scale off chip buffer memory 18). According to Haywood, the off chip buffer memory temporarily stores data packets when both head and tail FIFO memories are full, while during normal operation the tail FIFO memory stores temporarily overflows of data from the head FIFO memory and the head FIFO memory receives high speed data and transmitting the data to various switching element.

Applicant respectfully asserts that Haywood's variable size FIFO memory with head and tail caching is completely different in structure and function from Applicant's claimed features.

Further, Applicant respectfully asserts that Haywood is completely silent regarding deleting or adding of specific packet according to the result of monitoring as recited in Applicant's claimed invention. Although the Examiner cited col. 2, lines 13-15 and 20-22 of Haywood as describing steps of deleting and adding specific packets, Applicant cannot find any evidence of such features in the Examiner-cited portion of Haywood, or anywhere else in Haywood for that matter. Should the Examiner maintains the allegation that Haywood describes deleting or adding of specific packet according to the result of monitoring, Applicant would respectfully request the Examiner to be more specific in citing the disclosure of Haywood supporting the allegation.

Moreover, with respect to Jay's controlling clock frequency based on buffer level, Applicant respectfully submits that Jay is similar to a conventional method discussed in page 2 of the original specification, and that, even if Jay were combined with Haywood, the combination would still fail to arrive at Applicant's claimed invention, which includes controlling a stored packet quantity of the FIFO to delete a specified packet from an input side of the FIFO when the stored packet quantity exceeds a lower limit of the packet delete area, and to delete the packets when the stored packet quantity exceeds an upper limit of the packet delete area, and controlling the stored packet quantity of the FIFO to add a specified packet when the stored packet quantity falls below an upper limit of the packet add area, and to add the packets when the stored packet quantity falls below a lower limit of the packet add area, as recited amended claim 1.

Tokura generally describes a method for packet transfer that is controlled by using an acceleration rate of packet transfers. However, similar to Jay and Haywood, Tokura also fails to teach, disclose, or suggest controlling a stored packet quantity of the FIFO to delete a specified packet from an input side of the FIFO when the stored packet quantity exceeds a lower limit of the packet delete area, and to delete the packets when the stored packet quantity exceeds an upper limit of the packet delete area, and controlling the stored packet quantity of the FIFO to add a specified packet when the stored packet quantity falls below an upper limit of the packet add area, and to add the packets when the stored packet quantity falls below a lower limit of the packet add area, as recited in amended claim 1.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03, are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations.

Further, according to MPEP §2141(I), Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case. The Supreme Court in *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966), stated:

> Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented.

Moreover, according to MPEP §2141(II), when applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

> (A) The claimed invention must be considered as a whole;
>
> (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
>
> (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and
>
> (D) Reasonable expectation of success is the standard with which obviousness is determined.

As Jay, Haywood, and Tokura, combined or separately, fail to teach, disclose, or suggest each and every feature of claims 1-9 the obviousness rejection is improper.

In view of the amendment and arguments set forth above, Applicant respectfully requests the Examiner to follow tenets A-D in relying on Haywood, Jay, and Tokura in the obviousness rejection. Further, Applicant respectfully requests reconsideration and withdrawal of the §103(a) rejection of claims 1-9.

3. Rejections of claims 10-15 under 35 U.S.C. §103(a)

With respect to the rejection of independent claim 10 directed to a device and its dependent claims 12-15 under 35 U.S.C. §103(a) as being unpatentable over Jay and Haywood in view of Suzuki (U.S. 2002/0009054) or Oltean (US 6,044,113), Applicant respectfully traverses the rejection at least for the reasons set forth above with respect to claims 1-6 over Jay and Haywood, and for the reason that Suzuki and Oltean also fail to cure the deficiencies of Jay and Haywood.

Suzuki generally shows controlling a delay time of a packet by using a delay unit 103 in a device and method for reducing delay jitter in data transmission. Applicant respectfully asserts that there is no teaching, disclosure, or suggest of a FIFO, having an input side and an output side, that configures the jitter buffer, a packet deletion circuit provided on the input side of the FIFO, a packet addition circuit provided on the output side of the FIFO, a jitter buffer control circuit that includes a buffer accumulation level surveillance that monitors a stored packet quantity accumulated in the FIFO, a VCO that supplies to vary a reproduced clock frequency, and a buffer control circuit for controlling the operations of the FIFO and peripheral circuits thereof, wherein the buffer control circuit controls the quantity of packets accumulated in the FIFO to delete the packets when the stored packet quantity exceeds a lower limit of a packet delete area, and the buffer control circuit controls to add the packets when the stored packet quantity falls below an upper limit of a packet add area, and a decoder that accepts the packets outputted from the packet addition circuit, and decodes frames of the packets based on the clock frequency supplied from the VCO, as recited in amended claim 10 and its dependent claims.

Oltean, on the other hand, generally describes a digital pulse with modulator, which is completely different subject matter than the presently claimed invention and has no resemblance structurally or functionally to Applicant's device recited in claim 10 and its dependent claim 11.

Further, even if Suzuki or Oltean were combined with Jay and Haywood, the combination would still fails to include at least a packet deletion circuit provided on the input side of the FIFO, a packet addition circuit provided on the output side of the FIFO, a jitter

buffer control circuit that includes a buffer accumulation level surveillance that monitors a stored packet quantity accumulated in the FIFO, as recited in claim 10.

In view of the amendment and arguments set forth above, Applicant respectfully requests the Examiner to follow tenets A-D in relying on Haywood, Jay, Suzuki, and Oltean in the obviousness rejection. Further, Applicant respectfully requests reconsideration and withdrawal of the §103(a) rejection of claims 10-15.

Conclusion

In view of the amendments to the claims, and in further view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is requested that claims 1-2 and 4-15 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's representative, the Examiner is invited to contact the undersigned at the numbers shown.

Further, while no fees are believed to be due, the Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-4525.

Respectfully submitted,

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